

**REMARKS**

Claims 1-29 are pending in this application. By this Amendment, claims 1-5 and 14-18 are amended and claim 29 is added. No new matter is added. Reconsideration of the application based on the foregoing amendment and following remarks is respectfully requested.

**I. Allowable Subject Matter**

Applicant gratefully acknowledges the indication in the Office Action that claims 10 and 23 recite allowable subject matter. These claims are not rewritten in independent form, because it is believed that the base claims from which they depend are allowable as discussed below.

**II. Claim Rejections**

The Office Action rejects claims 1-9, 11-22 and 24-28 under 35 U.S.C. §102(e) over U.S. Patent No. 6,909,242 to Kimura; and rejects claims 2, 4, 15 and 17 under 35 U.S.C. §103(a) over Kimura. These rejections are respectfully traversed.

Claim 1 recites an electronic circuit that includes, among other features, a first circuit unit through which a first current having a first current level passes, and a second circuit unit to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element, at least one of the first circuit unit and the second circuit unit including a plurality of transistors connected in series or in parallel, respective gates of the transistors being mutually connected, the first circuit unit and the second circuit unit constituting a current mirror circuit.

Support for the above features may be found throughout the original specification and claims. For example, specific support may be found in the original specification and claims at least at paragraphs [0093], [0112], [0136], [0139], [0141], [0142].

The Office Action asserts that Kimura teaches the above combination of features with respect to Fig. 33C, 33A, 33C, 33A-D and at col. 40, lines 7-23. This is incorrect.

For example, none of the figures or text cited in the Office Action teach or suggest that the first circuit unit and the second circuit unit constitute a current mirror circuit, the first circuit unit and the second circuit unit including a plurality of transistors connected in series or in parallel, respective gates of the transistors being mutually connected.

As described in the original specification at least at paragraphs [0139] - [0142], by combining the above features, a circuit may be achieved that (1) allows the current level of the data current  $I_{data}$  to be set twenty five times greater than the driving current  $I_{el}$ , thereby allowing the data current  $I_{data}$  to be written to the storage capacitor  $C_n$  at a correspondingly higher speed; (2) improves the accuracy in the mirror characteristics; and (3) suppresses deterioration of the aperture ratio.

None of the circuits described in Kimura teach a circuit that includes the combination of features recited in claim 1. Accordingly, none of the circuits described in Kimura are capable of achieving the benefits that may be derived from such a circuit.

For at least these reasons, Kimura cannot reasonably be considered to teach or suggest all the features recited in independent claim 1. Independent claims 2-5 and 14-18 include features similar to those addressed above with respect to claim 1 and, therefore, Kimura cannot reasonably be considered to teach or suggest all the features recited in independent claims 2-5 and 14-18 for at least the reasons addressed above with respect to claim 1. Claims 6-13 and 19-28 depend from independent claims 1 and 14 and, therefore, Kimura cannot reasonably be considered to teach or suggest all the features recited in dependent claims 6-13 and 19-28 for at least the reasons addressed above with respect to claims 1 and 14 as well as for additional features that each of claims 6-13 and 19-28 recites.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-9, 11-22 and 24-28 under 35 U.S.C. §102(e) over Kimura; and the rejection of claims 2, 4, 15 and 17 under 35 U.S.C. §103(a) over Kimura are respectfully requested.

**III. New Claims**

Claim 29 is added. Support for claim 29 may be found in the original specification, starting at paragraph [0144], with respect to the circuit embodiment shown in Fig. 5.

None of the applied prior art references teach or suggest a circuit that includes the combination of components recited in claim 29 interconnected in the manner recited in claim 29.

**IV. Conclusion**

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-9, 11-22 and 24-29, in addition to the indicated allowable subject matter of claims 10 and 23, are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Attached:  
Request for Continued Examination

Date: January 12, 2007

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